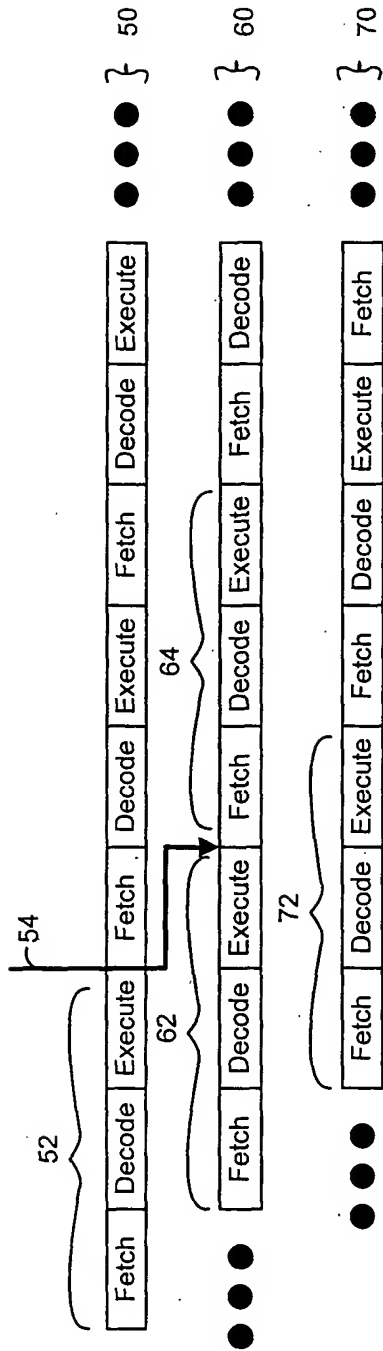


PRIOR ART
Fig. 1A



PRIOR ART
Fig. 1B

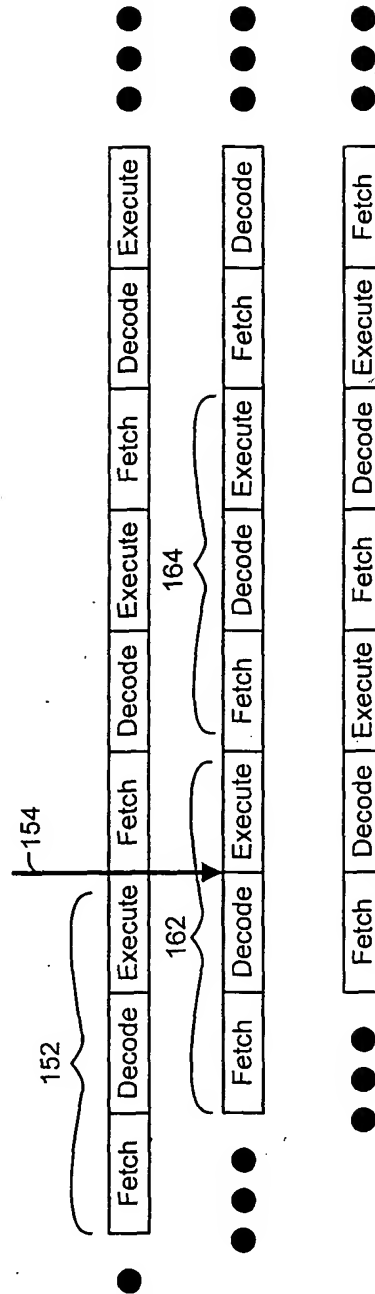


Fig. 2B

INPUT PIPELINE REGISTERS FOR A NODE IN AN ADAPTIVE COMPUTING ENGINE

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FIG. 2A-1
FIG. 2A-2
FIG. 2A

100

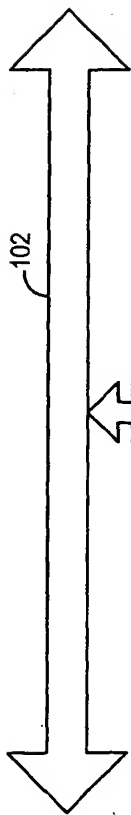
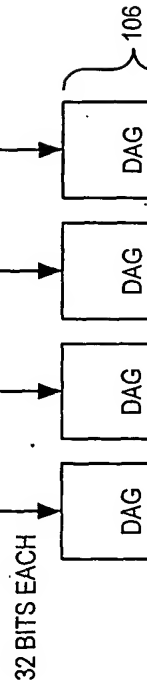


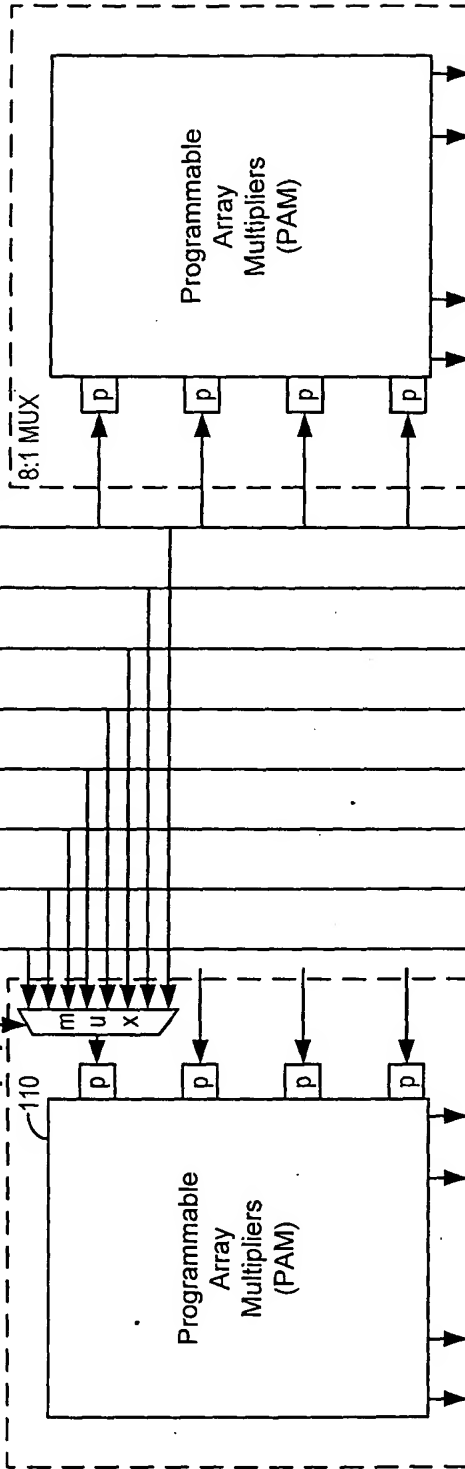
FIG. 2A-1



108

8:1 MUX
select
[2:0]

16 BITS EACH
8:1 MUX



INPUT PIPELINE REGISTERS FOR A NODE IN AN
ADAPTIVE COMPUTING ENGINE

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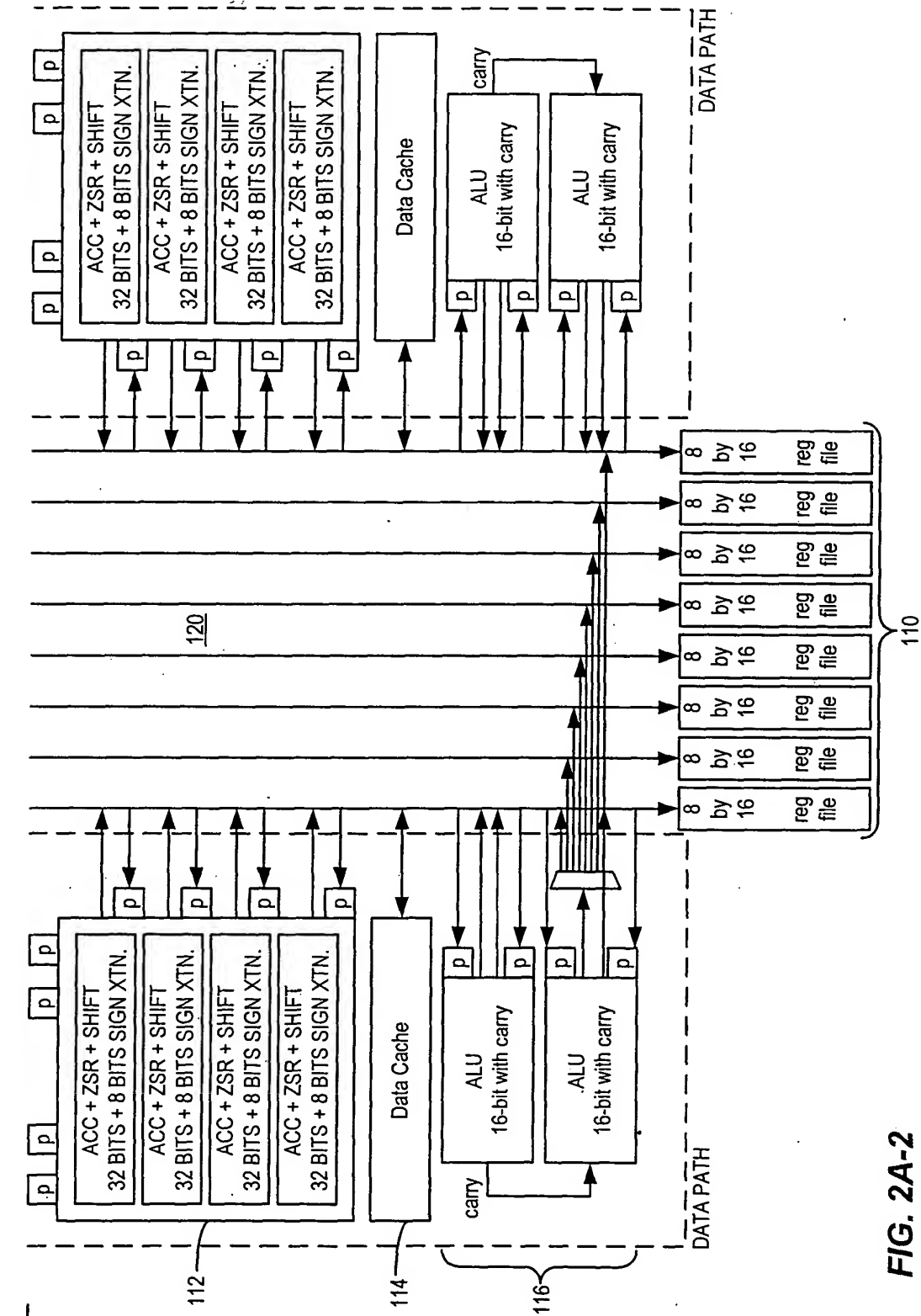


FIG. 2A-2

INPUT PIPELINE REGISTERS FOR A NODE IN AN
ADAPTIVE COMPUTING ENGINE

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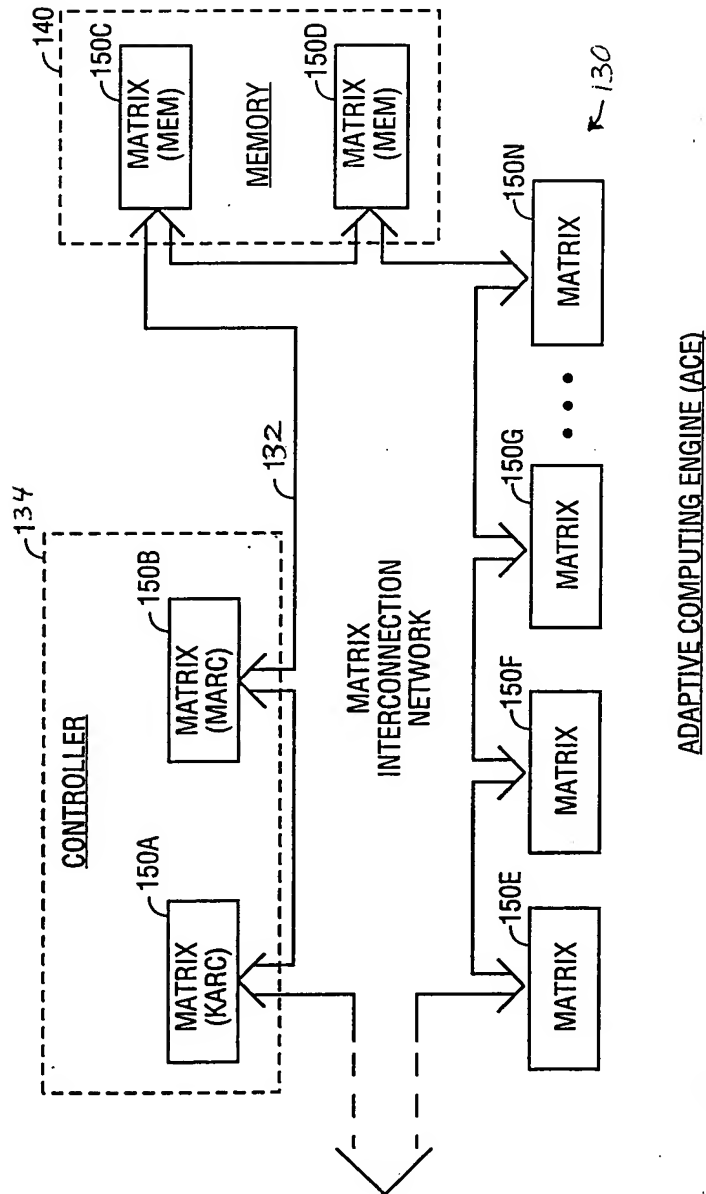


FIG. 3

INPUT PIPELINE REGISTERS FOR A NODE IN AN
ADAPTIVE COMPUTING ENGINE

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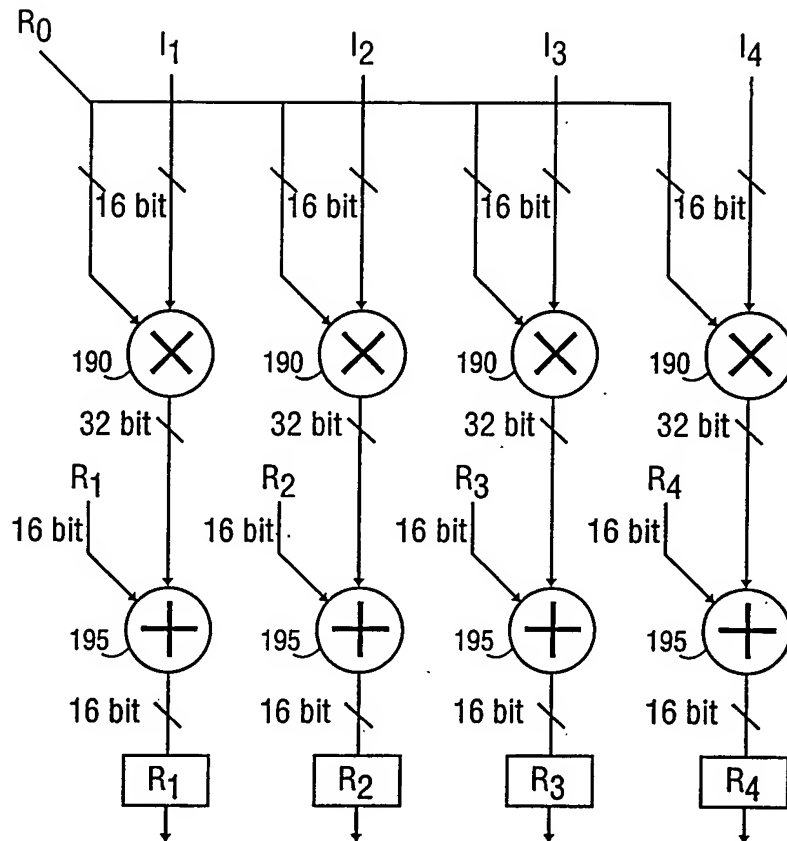


FIG. 4

INPUT PIPELINE REGISTERS FOR A NODE IN AN
ADAPTIVE COMPUTING ENGINE

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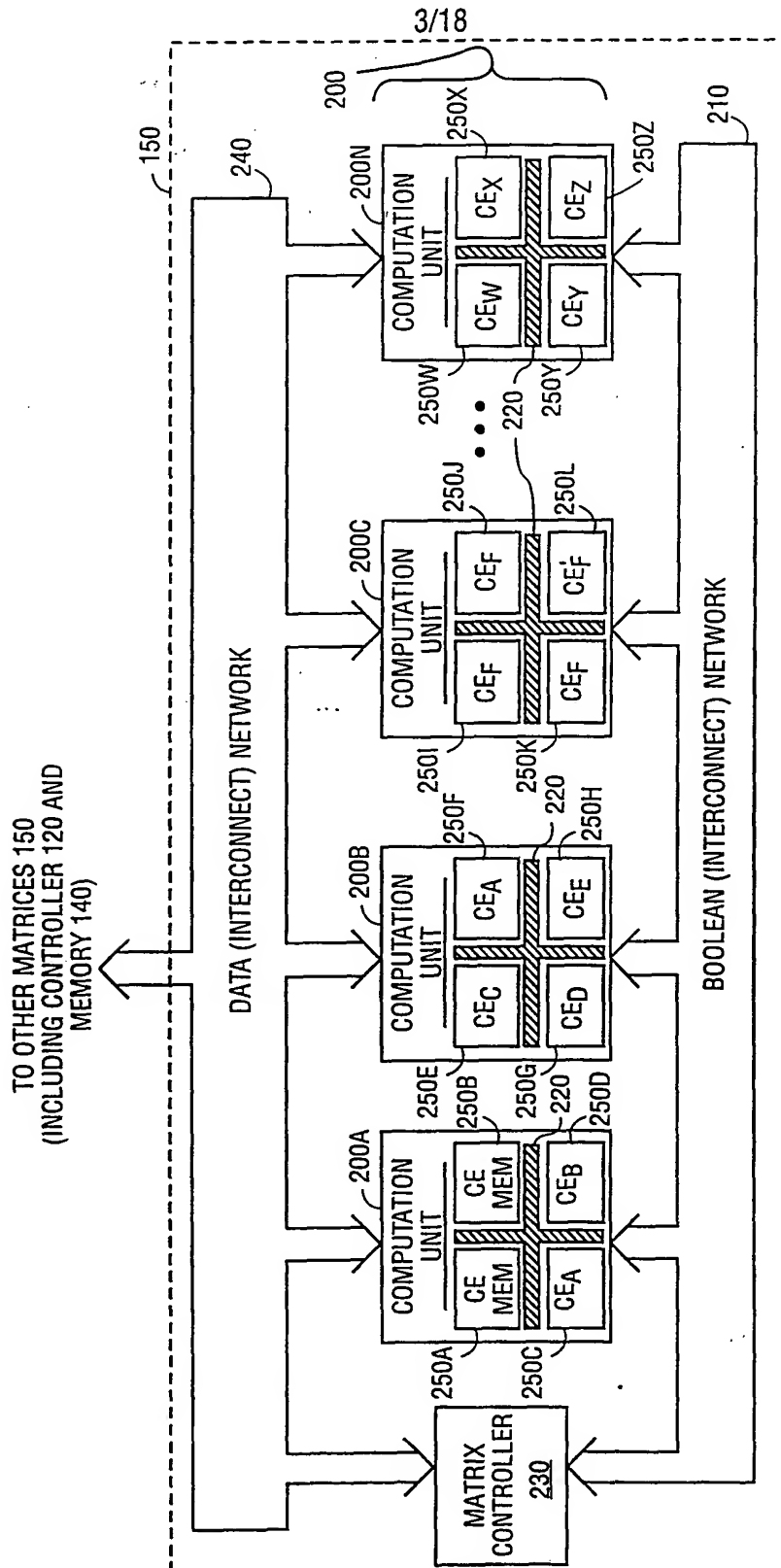


FIG. 5